TTXGEN 3.0
System Functional Specification

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1 Introduction

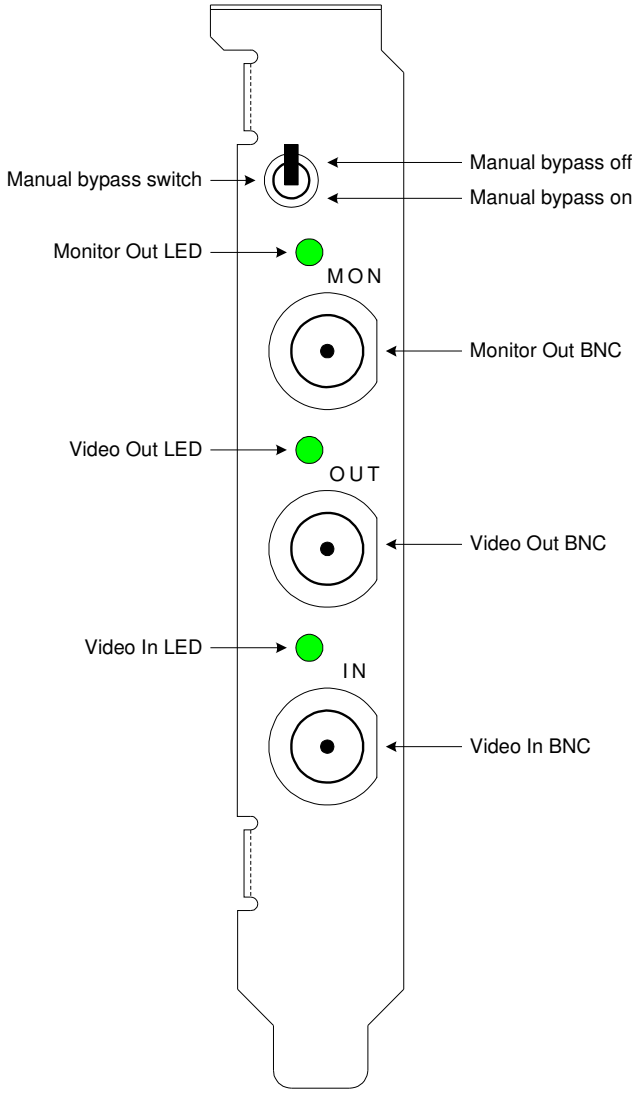
Polynesia/TTXGEN 3.0 is a teletext generator and video inserter on a PCI plug-in card for a personal computer. It is capable of generating teletext data for PAL 625-lines television systems according to the teletext standard World System Teletext (WST/625).

2 Features

TTXGEN 3.0 has been designed as the replacement to the legendary TTXGEN 2.1 ISA-card that has served small and medium-sized broadcasters for nearly a decade. TTXGEN 3.0 provides the following features:

- Half-length 32-bit Universal PCI-card compatible with both +5V and +3.3V PCI signaling standards prevalent in most modern personal computer.
- 3 BNC connectors and associated LEDs:
  - Video In: 1Vpp / 75 Ohm DC coupled
  - Video Out: 1 Vpp / 75 Ohm DC coupled
  - Monitor: 1 Vpp / 75 Ohm DC coupled. Provides a replicate of the signal on Video Out, but not subjected to the bypass mechanism (see below)
- Automatic bypass of Video Input to Video Output via electromechanical relay when no power is applied, or when the application software is not running. Bypass can also be invoked manually using a bypass switch, or by application software.
- Insertion of teletext data according to the WST/625 standard on line 6-22 (odd field) and 318-335 (even field). The lines to insert on are dynamically selected on a field-by-field basis (SW selectable).
- Teletext data are shaped with a 100% cosine-roll-off filter as specified by WST/625.
- Built-in broadcast quality video inserter so the generated teletext data can be inserted directly on a composite video baseband signal (CVBS). The video inserter can also be bypassed to provide the raw teletext data for an external video inserter/bridge directly on Video Out (SW selectable).
- The video source being inserted on can be either Video In or a built-in CVBS generator (SW selectable). The built-in CVBS generator generates a black video picture with no color information.
- DC-level restoration is performed on the video signal received on Video In to ensure the black level is at 0 V. The allowed range for the black level of the video signal received on Video In is –1.7 V to +1.3 V before DC-level restoration.
- Programmable insertion timing with a 36 ns resolution (SW selectable).
- Bypass relay for video path in case of power failure. Connects Video Out directly to Video In. The bypass relay can also be operated manually by a switch or by SW. The Monitor output is not operational when bypassing is activated.
- Field-upgradeable digital logic allows easy updates after deployment.
- Flexible PCI-interface with bus-master capabilities and large FPGA allows new features e.g. full-field teletext to be added.
- Support for PAL WST/525 or NTSC NABTS applications can be added through minor updates to the digital logic and modifications to the analog filtering and reference clock.

TTXGEN 3.0 provides the 3 BNC connectors, the 3 LED indicators and the bypass switch in the bracket on the back of the PCI card as shown in figure below:



▪ Figure 1: TTXGEN 3.0 bracket connections

The semantics of the 3 LED indicators are as follows:

- Monitor LED:
  - Off: card has not been activated by SW
  - On: card has been activated by SW
  - Blink: card has been activated by SW, but bypass is currently activated
- Video Out LED:
  - Off: not synchronized to selected video source
  - On: synchronized to selected video source and inserting teletext
  - Blink: synchronized to selected video source and not inserting teletext
- Video In LED:
  - Off: using internal CVBS generator
  - On: using Video In as video source
  - Blink: using Video In as video source, but failed to synchronize

3 Application programming interface

The application programming interface (API) has been designed to minimize the complexity of porting existing TTXGEN 2.1 teletext data drivers.

The user registers occupies a total of 16 bytes of memory mapped I/O. Additionally, the PCI controller uses another 256 bytes of memory-mapped I/O for it's own registers; furthermore, these registers are dual-mapped and can also be accessed through of 256 bytes of I/O ports.

The driver SW must dynamically determine the base address of the user registers; the operating system assigns the value to the card during the boot process.

3.1 TTXGEN 2.1 registers

TTXGEN 3.0 provides the following TTXGEN 2.1-compatible user accessible registers:

- Control register (8 bit read/write, offset 0)
    - Bit 0: 0: Disable. The card performs no insertion of teletext
      1: Enables. The card inserts teletext as instructed
    - Bit 1: 0 (reserved – TTXGEN 2.1 Full Field Operation)
    - Bit 2: 0: Use Video In as video source
      1: Use built-in CVBS generator as video source
    - Bit 3: 1 (reserved – TTXGEN 2.1 Shape Teletext Data)
    - Bit 4: 0: Use built-in video inserter
      1: Use external video inserter
    - Bit 5: 0: FIFO operates normally
      1: FIFO is held in reset state
    - Bit 6: 0: Don't force bypass relay on (i.e. force bypass of video signal)
      1: Force bypass relay on (i.e. do not force bypass of video signal)
    - Bit 7: 0 (reserved)

  The control register is reset to 0x08.
- Status register (8 bit read/write, offset 1)
    - Bit 0: 0: Not synchronized to selected video source
      1: Synchronized to selected video source
    - Bit 1: 0: Synchronization not lost
      1: Synchronization lost (sticky until cleared)
    - Bit 2: 0: Current field is even
      1: Current field is odd
    - Bit 3: 0: No FIFO underflow
      1: FIFO underflow (sticky until cleared)
    - Bit 4: 0: FIFO is non-empty
      1: FIFO is empty
    - Bit 5: 0: FIFO is non-full
      1: FIFO is full
    - Bit 6: 0: Bypass relay is not activated
      1: Bypass relay is activated
    - Bit 7: 0 (reserved – TTXGEN 2.1 External Video Field Indicator)

  To reset a sticky bit, write to the Status register with a 1 in the corresponding bit position, then write all zeroes to the Status register. Writing to the Status register also clears the interrupt request, if the originating condition has been removed.

- Extended Status Register (8 bit read-only, offset 2)

  Reading from this register returns the value 0xA9, indicating the product is suited for 625-line PAL systems (WST/625).
- FIFO Data Read register (8 bit read-only, offset 3)

  Reading from this register returns the data at the head of the 1 KB teletext data FIFO. This is for diagnostic reasons only, and should not be attempted while the card is enabled.
- FIFO Data Write register (8 bit write-only, offset 4)

  Writing to this register stores a byte at the tail of the 1 KB teletext data FIFO.
- FIFO Extended Data Write register (16 bit write-only, offset 4 and 5)

  Writing to this register stores two bytes at the tail of the 1 KB teletext data FIFO; the least significant byte is stored first.
- External Control register (8 bit write-only, offset 6)

  TTXGEN 3.0 does not implement this TTXGEN 2.1-specific register
- External Status register (8 bit read-only, offset 7)

  TTXGEN 3.0 does not implement this TTXGEN 2.1-specific register

3.2 Dynamic timing control

TTXGEN 3.0 provides 3 additional registers to support a new feature, dynamic digital control of the video insertion timing.

Each register contains an 11 bit timing value that determines when the timing event is taking place. Increasing this value will delay the timing events further, while decreasing it will make the timing event start earlier. By default these timing values correspond to nominal insertion of teletext on a nominal video signal, but they can be adjusted individually to suit special applications. Adjustment is best performed using an oscilloscope to measure and validate the effects. The timing value is measured in units of 1/27.75 MHz (~36.03 ns)

- Teletext multiplexer start timing (16 bit read/write, offset 8 and 9)
  - Bit 15-11: 0 (reserved)
  - Bit 10-0: Timing value defining when the teletext multiplexer will switch from the video source to the generated data. Default value of 235 corresponds to halfway between the end of a nominal color burst and the first bit of the teletext clock run-in
- Teletext multiplexer stop timing (16 bit read/write, offset 10 and 11)
  - Bit 15-11: 0 (reserved)
  - Bit 10-0: Timing value defining when the teletext multiplexer will switch from the generated data back to switch to the video source. Default value of 1737 corresponds to halfway between the last bit of teletext data and the end subsequent falling edge of the composite sync signal.
- Teletext data start timing (16 bit read/write, offset 12 and 13)
  - Bit 15-11: 0 (reserved)
  - Bit 10-0: Timing value defining when the insertion of the actual teletext data will begin. Default value of 258 corresponds to the teletext specification requirement that exactly 12.0 µs elapse from the falling edge of the composite sync pulse to the penultimate one-bit of the teletext clock run-in.

3.3 Interrupts

TTXGEN 3.0 uses a single interrupt line (known as INTA# in PCI terminology). An interrupt is generated when the teletext FIFO (see section 3.4) is empty. Normally this will happen after the end of each VBI interval, allowing driver SW almost a complete field period (~20ms) to react to the interrupt and provide new data to the teletext FIFO.

The maximum transmission rate is 315 Kbps (35 lines/frame), and data is being read from the teletext FIFO at a rate of at most 40.25 KBps (46 bytes per line).

The driver SW must dynamically determine which physical interrupt line is being used by the card; the operating system assigns the value to the card during the boot process.

3.4 Teletext FIFO

TTXGEN 3.0 incorporates a 1024-byte FIFO (*teletext FIFO*) that the teletext driver SW uses to provide dynamic VBI line control as well as the teletext data to insert. The driver SW writes data to this FIFO, and the teletext inserter logic reads the data in synchronism with the video signal as the VBI interval elapses.

The following VBI lines are available for insertion:

- Odd field: line 6-22 (17 lines)
- Even field: line 318-335 (18 lines)

Typically, at most line 7-22 and 320-336 are used for teletext (16 lines in each field).

For each VBI line available for insertion, a Line Header byte must be written to the teletext FIFO. The Line Header byte has the following format:

- Bit 0: 0: No insertion of teletext, use Video In for this line
  1: Insert teletext on this line
- Bit 1: 0 (reserved – TTXGEN 2.1 multiplexer select bit 2)
- Bit 2: 0: Line is in even field
  1: Line is in odd field
- Bit 3: 0: Blank this line (insert 0-data)
  1: 45 bytes follow with teletext data to insert
- Bit 4-7: 0000 (reserved)

Bit 2 determines which field the current Line Header belongs to. If the actual field doesn't match the selected field, no more insertions will be done in the current field, and insertion will restart in the next field that matches the selected field, presumably the following field (assuming fields are alternating, as is always the case unless an error has occurred).

Bit 3 must only be asserted if bit 0 is also asserted.

If bit 3 is asserted, 45 bytes of teletext data must follow the Line Header in the teletext FIFO. The first two bytes are the Clock Run-In (0x55 0x55), then comes the framing code (normally 0x27) and finally follows the 42 teletext data bytes. SW must perform all the required Hamming encoding and parity generation as TTXGEN 3.0 transmits the data bytes exactly as they are written to the teletext FIFO with no interpretation. The LSb of each byte is transmitted first.

If bit 3 is cleared, no data belonging to the current line follows the Line Header in the teletext FIFO. Blank (zero) data is inserted on the line (if bit 0 is asserted, otherwise the line is not modified).